REMARKS

Reconsideration and further examination are respectfully requested. Applicant has amended claim 1 to include the limitation of claim 2 and cancelled claim 2.

Rejections under 35 U.S.C. §103

Claims 1-7 were rejected under 35 U.S.C. §103(c) as being unpatentable over White (U.S. Patent No. 6,260,079) in view of Gavlik (U.S. Patent 6,745,325).

White:

White describes a fault-tolerant multi-peripheral-device enclosure for use in high availability systems (Abstract, White). The Examiner relies in particular on Figure 14 of White. The Examiner states:

"White discloses .... a plurality of serial bus controllers 1440, 1442 (see figure 14, co.. 23, lines 10-16); a serial bus 1438 coupled to the plurality of serial bus controllers 1440, 1442 (see figure 14, col. 23, lines 10-16), the serial bus for collecting environment ... and status information .... associated with one or more devices included in the enclosure... an arbitration mechanism for controlling access to the serial bus by the plurality of serial bus controllers (see col. 23, lines 48-67), the arbitration mechanism comprising a redundant control line 1502 (see col. 23, line 48 through col. 24 line 11)..."

Applicants respectfully disagree that White teaches the elements as alleged by the Examiner. As argued in the previous response, it is noted that elements 1440 and 1442 of White (PBC controller chips) are not *coupled to the serial bus* as recited in the claim. Rather, as stated in White, the serial bus is coupled to the processor 1436; communication with the serial bus is made possible through the processor (col. 23, lines 12-15). Accordingly, because the PBC controllers, do not even *touch* the serial bus, Applicants respectfully assert that it would be

impossible for the devices to *control* the serial bus, as recited in the claims of the present invention. It is noted that the serial bus controllers of the claims have the ability to *monitor* control lines associated with the serial bus and *drive* the control lines associated with the serial bus. Applicants respectfully maintain that *no equivalent structure of function* is provided by the PBC controllers of White.

The Examiner states, at page 4 of the office action: "... Applicants argue that White fail to teach the plurality of serial controller connected to the serial bus ... The Examiner does not agree. White et al. disclose controllers 1444 and 1446 (i.e., serial controller) connected to the serial bus 1438 (see figure 14, col. 23, lines 8-18). The controllers 1444 and 1446 is for collecting environmental and status information associated with one or more devices included in the enclosures..."

In view of the Examiner's response to Applicant's arguments, it appears that the Examiner's argument with regard to which elements of White teach the limitations of the claimed invention is different from the rejection of the claims provided by the Examiner. For example, in the rejection at page 2 of the Office Action, the Examiner identifies elements 1440 and 1442 as analogous to the serial bus controllers of the claims, but in the response to Applicant's arguments at page 4 of the office action, the Examiner identifies elements 1444 and 1446) as analogous to the claimed elements. Applicants respectfully request that the Examiner clarify the rejection of the claims to facilitate Applicant's response to the rejection.

Applicants will address both sets of elements in their response.

Elements 1440 and 1442 of White are port bypass circuit controllers. The port bypass circuit controllers are coupled to a port bypass circuit bus 1432 which is further coupled to a FC

loop indicated in FIG. 14 by the heavy line, which interconnects port bypass circuits 1422, 1423. (see col. 22, lines 63-66).

White states, at column 23, lines 12-16:

"... The LCC contains a processor 1436, which runs an enclosure services process and other control programs. *This processor 1436 includes circuitry that implements an FC port as well as ports to three different internal busses.* One of the internal bussess 1438, in a preferred embodiment an I2C bus, interconnects the processor 1436 with PBC controller chips 1440 and 1442 and with other components such as temperature sensing devices and power monitoring devices 1444 and 1446..."

Thus, as clearly stated in White, *the processor 1436 implements the port to the I2C bus.* There simply is no shared *control* of or *arbitration for* the I2C bus disclosed or suggested by White. In fact, the PBC controller 1440 and 1442 are not even coupled to the I2C bus; rather, they are coupled to the Fibre Channel link, and are used for controlling the port bypasses on the Fibre Channel link.

The Examiner states at page 4 that elements 1444 and 1446 also disclose 'serial bus controllers...' However, such a limitation is neither taught nor suggested by White. Rather, the only reference to these elements is at column 23 lines 16 and 17, where they are described respectively as 'temperature sensing devices' and 'power monitoring devices...' There is simply no mention or suggestion in White that these devices control the I2C bus. In fact, such a conclusion is the *opposite* as to what is actually stated in White, which is that the LCC processor 1436 "includes circuitry that implements ... ports to three different internal busses...One of the internal busses ... an I2C bus..."

Thus White describes a centralized control of the I2C bus at the processor 1436.

The Examiner admits, on page 3 of the office action:

"... White does not specifically disclose wherein each of the plurality of serial bus controllers is assigned a different number n of a period td for driving the control signal after a delay t1 when seeking to take control of the serial bus. However, Gavlik discloses the serial interface controller comprising each of the plurality of serial bus controllers is assigned a different number n of a period td for driving the control signal after a delay t1 when seeking to take control of the serial bus (see col. 8, line 27 through col. 9 line 35). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Gavlik into the teachings of White because the failure of any microcontroller does not prevent any other microcontroller from being programmed and also provide full autonomous programming of multiple microcontrollers via a 2-wire interface..."

Actually, Gavlik describes, at col. 8 lines 27 – 36:

"... After a reset event ... occurs, microcontroller 21 monitors the SCL line and the SDA line during a predetermined time period to determine if another microcontroller acts as a server. If not, the microcontroller 211 will act as a server at the end of the predetermined time period..." where the predetermined time periods are determined by the address values set by address resistor matrices.

Thus, rather than 'driving control lines' for different time periods, as stated in the claims of the present invention, Gavlik describes only that each microprocessor *waits* for a different predetermined time period before accessing the control lines.

One the control lines are accessed, it would appear that each microcontroller then drives control lines for a fixed period of time (12.6 microseconds for the server routine, for example).

Thus, the arbitration scheme of Gavlik, where each microprocessor waits different time periods before controlling bus signals is distinctly different from that of the claimed invention, where each serial bus controller "... is assigned a different number n of a period td for driving the control signals after a delay t1 when seeking to take control of the serial bus..."

For at least the reasons described above, Applicants disagree with the Examiner's conclusions with regard to the combination of White and Gavlik, and respectfully submit that the combination fails to satisfy the burden for establishing a prima facie case of obviousness with regard to the claims of the present invention. As described in M.P.E.P. §2143, 'To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations..."

No motivation for the modification suggested by the Examiner

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

"Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." Dembiczak, 175 F.3d at 999; see also Ruiz, 234 F.3d at 665 (explaining that the temptation to engage in impermissible hindsight is especially strong with seemingly simple mechanical inventions). This is because

"[c]ombining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight." Dembiczak, 175 F.3d at 999. Therefore, we have consistently held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings *in the particular manner claimed*. See, e.g., In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000). [Emphasis added by the Applicant]

It is the Examiner's position that one would be motivated to modify White to incorporate the teachings of Gavlik because 'the failure of any microcontroller does not prevent any other microcontroller from being programmed and also provide full autonomous programming of multiple microcontrollers via 2-wire interface...'

Applicants disagree that one would be motivated to modify White to incorporate the programming description of Gavlik for at least the reason that it is unclear exactly what structures of White the Examiner is attempting to program; as described above, the elements that are coupled to the serial bus are 'temperature sensing devices' and 'power monitoring devices,' it is unclear as to why White would seek to program such devices.

In addition, and as described above, one must be motivated to combine the references *in the particular manner claimed*. Applicants cannot see how the motivation provided by the Examiner would lead one of skill in the art to combine the references in the particular manner claimed, in particular for the reason that White does not disclose or suggest a distributed control mechanism for the I2C bus. To suggest that White may be altered from its described state, where the LCC processor 1438 controls the ports of the I2C bus to one where the control is distributed would only serve to complicate White with no apparent advantage.

In response to Applicant's argument, the Examiner states, at page 4 "...In this case, the combination of references White and Gavlik..." but fails to say where the teaching or suggestion can be found in the references.

Applicants further submit that the two references are from two different arts, concerned with two different ideas; Gavlik is concerned with forwarding a replacement program into a network interface card. White is concerned with providing a fault tolerant enclosure. The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983). Applicants can find no advantage from the combination of White with Gavlik.

The Examiner states, at page 4 that 'the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. Ex parte Obiaya 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985)." Applicants fail to see how the complete modification of the I2C bus control in White from a centralized controller to a distributed controller in a manner of the claimed invention 'naturally flows' from the prior art, which discloses only the combination of a centralized controller of an I2C bus and a manner of distributing a computer program to microprocessors.

In addition, it is well known that a "... prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). Gavlik, which

seeks to program micro-proccessors is from a different field of endeavor and not reasonably pertinent to the particular problem with which the Applicant is concerned.

For the several reasons outlined above it is respectfully submitted that there is no motivation for the combination of references suggested by the Examiner, and therefore a prima facie case under 35 U.S.C.§103 has not been established. It is therefore requested that the rejection be withdrawn.

Combination neither describes or suggests the claimed invention

However, even if a motivation for combining the references could be found, Applicants note that the combination of references still fails to disclose every element of the claims. Although the Examiner has stated, at page 4 of the office action that 'In response to applicant's arguments against the references individually, one cannot show non-obviousness by attacking references individually where the rejections are based on combination of references...' Applicant respectfully notes that they have not attacked the references individually, although they have endeavored to show that the elements relied on by the Examiner as teaching various claimed elements lack the structure and functionality to meet the limitations of the claims. Applicants have then *only* argued the references in combination. However, if *neither* of the references show *any* of the limitations, it is not possible that the combination of the references teach the invention as claimed.

For example, neither White, nor Gavlik, alone or in combination, describe "serial bus controllers... for collecting environmental and status information associated one or more devices included in the enclosure ..." As noted above, White describes a centralized serial bus controller, not a plurality of serial bus controllers as claimed. Gavlik neither describes nor suggests a serial

bus controller. Thus the combination of references fails to teach, describe or suggest this limitation.

The Examiner admits that White does not teach or describe the arbitration mechanism as claimed. As described above, Gavlik neither teaches or describes the arbitration mechanism as claimed. Accordingly, the combination of references neither teach nor describe the claimed arbitration mechanisms.

Therefore for at least the reason that the combination of Gavlik and White fail to teach several limitations of the claims, it is requested that the rejection of claim 1 be withdrawn. Dependent claim 3 serves to further limit claim 1 and are allowable for at least the same reason as claim 1.

Claim 4 recites "...providing a serial bus coupled to a plurality of serial bus controllers, the serial bus for propagating environmental and status information between one or more devices in the enclosure , *wherein each of the serial bus controllers is coupled to the serial bus by one of a plurality of redundant control lines* ... arbitrating for access to the serial bus by the plurality of serial bus controllers by allocating a different number n of a period td to each one of the serial bus controllers of the plurality, wherein each of the serial bus controllers ***drives their associated control line by their for a time period equal to n*td*** *to gain control of the serial bus* ..."

Accordingly, for at least the reason that the combination of White and Galvin fails to describe or suggest several limitations of claim 4 that are similar to claim 1 (i.e., 'a serial bus coupled to a plurality of serial bus controllers.... arbitrating for access ... by allocating a different number n of a period td to each one of the serial bus controllers), it is requested that the rejection be withdrawn. Claims 5-7 serve to further limit claim 4 and are allowable for at least the same reasons as claim 4.

Conclusion:

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at the number listed below so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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